## DETAILED ACTION

### Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 25, 2009 has been entered.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with DOUGLAS HOLTZ on February 14, 2011.

The application has been amended as follows:

In the Claims:

"and" (claims 1 and 2, line 12) has been deleted.

"portion" (claims 1 and 2, last line) has been changed to: --portion and detachably holds the printed circuit board at said non-conductive portion, and said weak-adherence adhesive pattern has a plurality of thickness regions differing in thickness from the surface of said plate according to thickness regions of the printed circuit board--.

"The holding and conveyance jig according to claim 2, wherein a non-adhesive pattern is formed at a position correspon\ding to said conductive portion on the surface of said weak-adherence adhesive layer" (claim 5, lines 1-4) has been changed to: --A holding and conveyance jig for detachably holding and conveying a printed circuit board on which electronic components are mounted, said jig comprising: a plate which has a weak-adherence adhesive layer on a surface of the plate; wherein: said printed circuit board has a conductive portion and a non-conductive portion on a surface of the printed circuit board, said printed circuit board is placed and held on the surface of said plate, a non-adhesive pattern is formed at a position corresponding to said conductive portion on the surface of said weak-adherence adhesive layer, said weak-adherence adhesive layer detachably holds the printed circuit board at said non-conductive portion, and said weak-adherence adhesive layer has a plurality of thickness regions differing in thickness from the surface of said plate according to thickness regions of the printed circuit board--.

"placed by" (claim 6, line 13) has been changed to: --placed and held by--.

"pattern" (claim 6 last line) has been changed to: --pattern, wherein said weak-adherence adhesive pattern has a plurality of thickness regions differing in thickness from the surface of said plate of the jig according to thickness regions of the printed circuit board

Claims 3, 16, 18 and 19 have been canceled.

3. The following is an examiner's statement of reasons for allowance: the prior art of record fails to teach or suggest the jig for detachably holding and conveying a printed circuit board on which electronic components are mounted including "the weak-adherence adhesive pattern is

formed at portion corresponding to the non-conductive portion and detachably holds the printed circuit board at said non-conductive portion, and said weak-adherence adhesive pattern has a plurality of thickness regions differing in thickness from the surface of said plate according to thickness regions of the printed circuit board" in combination with other limitations as recited in claims 1, 2, 5 and 6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONGHAI D. NGUYEN whose telephone number is (571)272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derris H. Banks can be reached on (571)-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN
February 14, 2011

/Donghai D. Nguyen/
Primary Examiner, Art Unit 3729